REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
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REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34
REV STATUS				REV																
OF SHEETS				SHEET			1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A	PREPARED BY Kenneth Rice	**DEFENSE SUPPLY CENTER COLUMBUS** **COLUMBUS, OHIO 43216** **http://www.dscc.dla.mil**
STANDARD MICROCIRCUIT DRAWING THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE AMSC N/A	CHECKED BY Rajesh Pithadia	
	APPROVED BY Raymond Monnin	MICROCIRCUIT MEMORY CMOS, DIGITAL, 256M X 8 Bit STACKED DIE (2Gbit) SYNCHRONOUS DRAM (SDRAM), MODULE
	DRAWING APPROVAL DATE 03 – 02 – 07	
	REVISION LEVEL	SIZE A / CAGE CODE **67268** / **5962-02518**
		SHEET 1 OF 34

DSCC FORM 2233
APR 97

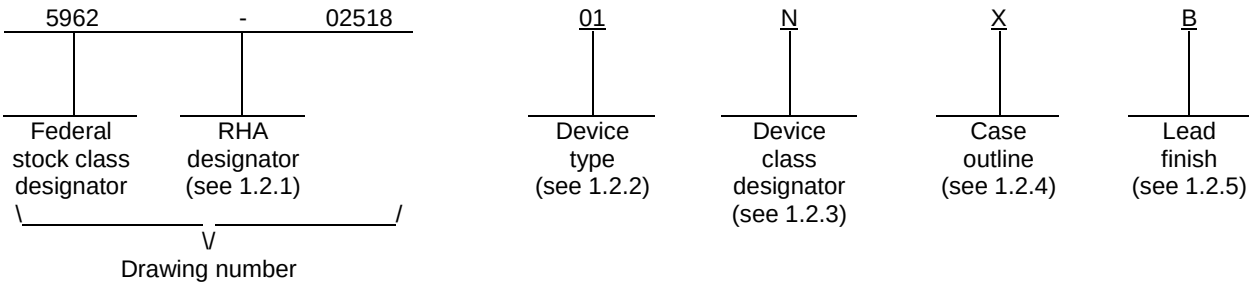
5962-E369-02

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

1.1 Scope. This drawing documents three product assurance class levels consisting of space application (device Class V), high reliability (device class Q), and nontraditional performance environment (device Class N). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN. **For device Class N, the user is cautioned to assure that the device is appropriate for the application environment.**

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device Classes N, Q, and V RHA marked devices meet the MIL-PRF- 38535 specified RHA levels and are marked with appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify 128M x 8 bit SDRAM circuits utilizing vertical stacking technology as follows:

Device Type	Generic Number	Circuit Function	No. Die in Stack
01	SD256Mx88	16M x 8 bit x 16 bank, synchronous DRAM (2 Gbit)	8 Dice

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device Class	Device Requirements Documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN Class Level B microcircuits in accordance with MIL-PRF-38535, Appendix A **1/**
N	Certification and qualification to MIL-PRF-38535 for plastic encapsulated microcircuit (PEM). **2/**
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline Letter	Descriptive Designator	Terminals	Package Style
X	See figure 1	54	Plastic small outline package

1.2.5 Lead Finish. The lead finish is as specified in MIL-PRF-38535 for device Classes N, Q, V.

1/ For this drawing, device class M shall not apply.

2/ A device outside the traditional performance environment; a plastic encapsulated microcircuit (PEM).

1.3 Absolute maximum ratings. 3/ 4/

Supply voltage range, (V_{CC})	-0.5 V dc to +4.6 V dc
Voltage range on any input pin	-0.5 V dc to +4.6 V dc
Voltage range on any output pin	-0.5 V dc to Vcc +0.5 V dc
Short-circuit output current	50 mA
Power dissipation	2 W
Operating free-air temperature range, (T_A)	-40°C to +85°C
Storage temperature range, (T_{SIG})	-55°C to +125°C
Thermal resistance, junction-to-case, (θ_{JC}):	
Case X	15°C/W

1.4 Recommended operating conditions.

Supply voltage range, (V_{CC})	+3.0 V dc to +3.6 V dc
Supply voltage, (V_{SS})	0 V dc
High-level input voltage, (V_{IH})	+2.0 V dc to Vcc +0.3 V dc
Low-level input voltage, (V_{IL})	-0.3 V dc to +0.8 V dc
Operating free-air temperature range, (T_A)	-40°C to +85°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

4/ All voltage values in this drawing are with respect to V_{SS}

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device Classes N, Q, and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit or function as described herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes N, Q and V.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.2.4 Block or logic diagram(s). The block or logic diagram(s) shall be as specified on figure 4.

3.2.5 Timing waveforms. The timing waveforms shall be as specified on figure 5.

3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in Table IIA. The electrical tests for each subgroup are defined in Table I.

3.4.1 Functional Tests. Listed below is a set of required test patterns to be used in conjunction with table I for the functional tests of Subgroups 7 and 8 as well as the A.C. parametric tests in Subgroups 9, 10 and 11. These tests have been determined to effectively stress sensitivities related to address and data pattern as well as functionally test the device to be supplied to this specification. A.C. parametric limits are tested by using the limit values as input conditions and measurement delays of the timing sets associated with Subgroups 7 and 8. Additional test patterns may also be used.

a.	Walking 0101 Pattern	Full Page Burst / Sequential (Vmin)
b.	Walking FEFE Pattern	Full Page Burst / Sequential Vmax)
c.	March 00/FF Pattern	8 Byte Burst / Interleave (Vmin)
d.	March FF/00 Pattern	8 Byte Burst / Interleave (Vmax)
e.	March AA/55 Pattern	8 Byte Burst / Interleave (Vmin)
f.	March 55/AA Pattern	8 Byte Burst / Interleave (Vmax)
g.	March FF/00 Pattern	1 Byte Burst / Sequential (Vmin)
h.	March 00/FF Pattern	1 Byte Burst / Sequential (Vmax)
i.	March 66/33 Pattern	1 Byte Burst / Sequential (Vmin)
j.	March 33/66 Pattern	1 Byte Burst / Sequential (Vmax)
k.	Refresh Pause Checkerboard	(Vmin)
l.	Refresh Pause Checkerboard	(Vmax)
m.	Refresh Pause Checkerboard Bar	(Vmin)
n.	Refresh Pause Checkerboard Bar	(Vmax)

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes N, Q, and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes N, Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes N, Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes N, Q, and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes N, Q, and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

4.QUALITY ASSURANCE PROVISIONS.

4.1 Sampling and inspection. For device Classes N, Q, and V, sampling and inspection procedure shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device Classes N, Q, and V screening shall be in accordance with MIL-PRF-38535, the manufacturer's QM plan, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes N, Q, and V.

a. Temperature and voltage accelerated burn-in shall be employed for the SDRAM. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(1) T_A = +135°C, V_{CC} = 4.0V
(2) Test duration: 72 hours for classes N & Q, and 100 hours for class V.

b. Interim and final electrical test parameters shall be as specified in Table IIA herein.

(1) Temperature and voltage accelerated dynamic burn-in (Method 1015 of MIL-STD-883, Test Condition D).

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.2.2 Additional criteria for device class N.

a. Temperature cycling per Method 1010, condition B, 10 cycles.

b. Post burn-in PDA is 5% maximum for subgroups 1 and 7 failures.

4.3 Qualification inspection for device classes N, Q, and V. Qualification inspection for device classes N, Q, and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes N, Q, and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein and the QM Plan.

4.4.1 Group A inspection.

a. Group A testing is not required if all tests have been performed during final electrical of the 100% Screening test. See footnote 7/ for Table IIA.

b. Subgroup 4 (capacitance measurements) shall be measured only for initial qualification and after any process or design changes, which may affect input or output capacitance. Capacitance shall be measured between the designated terminal and GND at a frequency of 1 MHz. Sample size is 5 devices with no failures, and all input and output terminals tested.

c. For device Classes N, Q, and V, subgroups 7 and 8 shall include verifying the functionality of the device.

Table I. Electrical Performance Characteristics

Test	Symbol	Test Conditions 1/ -40°C ≤ T_A ≤ +85°C +3.135V ≤ V_{CC} ≤ +3.465V unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
High-level output voltage	V_{OH}	I_{OH} = -2mA	1,2,3	All	2.4		V
Low Level output voltage	V_{OL}	I_{OL} = +2mA	1,2,3	All		0.4	V
Input Current (leakage)	I_I	0V ≤ V_I ≤ V_{CC} All other pins = 0V to V_{CC}	1,2,3	All		±10	µA
Output current (leakage)	I_O	0V ≤ V_O ≤ V_{CCQ} Output disabled	1,2,3	All		±10	µA
Average read or write current	I_{CC1}	Burst length = 1 t_{RC} ≥ t_{RC} MIN, I_{OH}/I_{OL} = 0mA, One bank activated 2/ Inactive die are in I_{CC2P}	1,2,3	All		450	mA
Precharge standby current in power-down mode	I_{CC2P}	CKE ≤ V_{IL}MAX, t_{CK} = MIN 3/	1,2,3	All		20	mA
	I_{CC2PS}	CKE & CLK ≤ V_{IL}MAX, t_{CK} = ∞ 4/	1,2,3	All		10	mA
Precharge standby current in non power-down mode	I_{CC2N}	CKE ≥ V_{IH}MIN, t_{CK} = MIN 3/	1,2,3	All		150	mA
	I_{CC2NS}	CKE ≥ V_{IH}MIN, CLK ≤ V_{IL}MAX, t_{CK} = ∞ 4/	1,2,3	All		75	mA
Active standby current in power-down mode	I_{CC3P}	CKE ≥ V_{IL}MAX, t_{CK} = MIN One bank activated 3/	1,2,3	All		50	mA
	I_{CC3PS}	CKE & CLK ≤ V_{IL}MAX, t_{CK} = ∞ One bank activated 4/	1,2,3	All		50	mA
Active standby current in non power-down mode	I_{CC3N}	CKE ≥ V_{IH}MIN, t_{CK} = MIN One bank activated 3/	1,2,3	All		300	mA
	I_{CC3NS}	CKE ≥ V_{IH}MIN, CLK ≤ V_{IL}MAX, t_{CK} = ∞, One bank activated 4/	1,2,3	All		200	mA
Burst current	I_{CC4}	Continuous burst, I_{OH}/I_{OL} = 0mA, 5/ All banks activated t_{CC} = clocks inactive die are in I_{CC2P}	1,2,3	All		450	mA
Refresh Current	I_{CC5}	t_{RC} ≥ t_{RC}MIN	1,2,3				mA
		2 Die		All		500	
		4 Die		All		1000	
		8 Die		All		2000	
Self Refresh Current	I_{CC6}	CKE < 0.2V	1,2,3	All		30	mA
Input capacitance, CLK input	$C_{I(S)}$	f = 1MHz, bias on pin under test = 0V, all other pins are open, T_A=+25°C, See 4.4.1b 6/	4	All		35	pF
Input capacitance, address and control inputs: A0 – A11, /WE, /CS, DQMx, /RAS, /CAS, BA0, BA1	$C_{I(AC)}$		4	All		60	pF
Input capacitance, CKE input	$C_{I(E)}$		4	All		30	pF
Output capacitance	C_O		4	All		40	pF

See footnote at end of table.

Table I. Electrical Performance Characteristics – continued

Test	Symbol	Test Conditions 1/ -40°C ≤ T_A ≤ +85°C +3.135V ≤ V_{CC} ≤ +3.465V unless otherwise specified	Group A Subgroups	Device Type	Limits		Unit
					Min	Max	
Functional test		See 4.4.1c	7,8A,8B	All	L	H	
Cycle time, CLK (system clock)	t_{CC}	See figures 4 and 5. 7/	9,10,11	All			ns
		Read latency = 2			12	1000	
		Read latency = 3			10	1000	
Pulse duration, CLK (system clock) high	t_{CH}	See figures and 4 and 5. 7/	9,10,11	All	3		ns
Pulse duration, CLK (system clock) low	t_{CL}		9,10,11	All	3		ns
Access time, CLK ↑ to data out	t_{SAC}	See figures and 4 and 5. 7/ 8/	9,10,11	All			ns
		Read latency = 2				6	
		Read latency = 3				6	
Delay time, CLK to DQ in the low-impedance state	t_{SLZ}	See figures 4 and 5. 7/ 9/	9,10,11	All	0		ns
Delay time, CLK to DQ in the high-impedance state	t_{SHZ}	See figures and 4 and 5. 7/ 10/	9,10,11	All			ns
		Read latency = 2			3	7	
		Read latency = 3			3	7	
Setup time, data input	t_{SS}	See figure 4 and 5. 7/	9,10,11	All	2		ns
Setup time, address	t_{AS}	See figures 4 and 5. 7/	9,10,11	All	2		ns
Setup time, control input (/CS, DQMx, /RAS, /CAS, /WE)	t_{CS}		9,10,11		2		ns
Setup time, CKE (suspend entry/exit, power-down entry)	t_{CES}		9,10,11		2		ns
Hold time, data input	t_{SH}		9,10,11		1		ns
Hold time, address	t_{AH}		9,10,11		1		
Hold time, control input (/CS, DQMx, /RAS, /CAS, /WE)	t_{CH}		9,10,11		1		
Hold time, CKE	t_{CEH}		9,10,11		1		
Row Cycle Time	t_{RC}		9,10,11		70		
Row Active Time	t_{RAS}		9,10,11		0.05	100	µs
/RAS to /CAS	t_{RCD}	See figures 4 and 5. 7/ 11/	9,10,11	All	20		ns
Row precharge time	t_{RP}	See figures 4 and 5. 7/	9,10,11	All	20		ns
Final data in to Row Precharge	t_{RDL}		9,10,11	All	12		ns
Last data in to new column address delay	t_{CDL}	See 4.2.5	9,10,11	All	1		CLK
Last data into burst stop	t_{BDL}	See 4.2.5	9,10,11	All	1		CLK
Column Address to Column Address delay	t_{CCD}	See 4.2.5	9,10,11	All	1		CLK
Row active to row active delta	t_{RRD}		9,10,11	All	20		ns
Transition time, all inputs	t_R	See figures 4 and 5. 7/ 12/	9,10,11	All		10	ns
Refresh interval	t_{REF}	See figures 4 and 5. 7/	9,10,11	All		128	ms

See footnotes at end of table.

TABLE I. Electrical performance characteristics – continued

1/ All specifications apply to the device after power-up initialization. All control and address inputs must be stable and valid.
Subgroup 1, 4, 7 and 9 are tested at T_A = 25°C
Subgroup 2, 8A and 10 are tested at T_A = 85°C
Subgroup 3, 8B and 11 are tested at T_A = -40°C
2/ Control and address inputs change state only twice during t_{RC}.
3/ Control and address inputs change state only once every 2 x t_{CK}.
4/ Control and address inputs do not change (stable).
5/ Control and address inputs change state only once every cycle.
6/ This test is performed at initial characterization and after any design or process changes.
7/ All references are made to the rising transition of CLK unless otherwise specified.
8/ t_{AC} is referenced from the rising transition of CLK that precedes the data-out cycle. For example, the first data out t_{AC} is referenced from the rising transition of CLK that is one cycle before read latency for the READ command. An access time is measured at output reference level 1.4V.
9/ t_{LZ} is measured from the rising transition of CLK that is one cycle before read latency for the READ command.
10/ t_{HZ} (max) defines the time at which the outputs are no longer driven and is not referenced to output voltage levels.
11/ For read or write operations with automatic deactivate, t_{RCD}, must be set to satisfy minimum t_{RAS}.
12/ Transition time (rise and fall) should be a minimum of 1 ns and a maximum of 5 ns measured between VIHMIN and VILMAX. This is ensured by design but not tested.

4.4.2 Group C Inspection. The group C inspection end-point electrical parameters shall be as specified in Table IIA herein..

4.4.2.1 Additional criteria for device Classes N, Q, and V. Temperature and voltage accelerated life test shall be employed for the SDRAM. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883. The total number of die used determines the sample size. For example, device 01 contains 8 dice so the number of sample will be 6 (45÷8≈6) modules.

a. T_A = +135°C, V_{CC} = 4.0V
b. Test duration: 400 hours

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in Table IIA herein.

a. Subgroups 4, 6, and 8 of Table V of MIL-PRF-38535 do not apply to class N devices.

b. For class N devices, a biased Highly-Accelerated Temperature and Humidity Test (HAST) will be added as Subgroup 9 to Group D. Duration will be 96 hours at 130°C, 85% Relative Humidity with bias set at 110% of rated operating voltage. Sample size is 5 modules with zero rejects allowed.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in Table IIA herein.

b. For device classes N, Q, and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the post-irradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in Table IIA herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

TABLE IIA. Electrical Test Requirements. 1/ 2/ 3/ 4/ 5/ 6/ 7/

Line Number	Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)		
		Device Class N	Device Class Q	Device Class V
1	Interim electrical parameters	1, 7	1, 7	1, 7, 9
2	Static burn-in 1 and 2 (Method 1015)	Not required	Not required	Required
3	Interim electrical parameters (post static burn-in	- - -	- - -	1*, 7*, Δ
4	Dynamic burn-in (Method 1015)	Required	Required	Required
5	Interim electrical parameters (post dynamic burn-in			1*, 7*, Δ
6	Final electrical parameters	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
7	Group A test requirements	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11	1, 2 , 3 ,4** , 7, 8A, 8B, 9, 10, 11	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
8	Group C end-point electrical parameters	1, 2, 3, 7, 8A, 8B, 9, 10, 11	1, 2, 3, 7, 8A, 8B	1, 2, 3, 7, 8A, 8B, 9, 10 , 11 Δ
9	Group D end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9
10	Group E end-point electrical parameters	1, 7, 9	1, 7, 9	1, 7, 9

1/ Blank spaces indicate tests are not applicable.

2/ Any or all subgroups may be combined when using high-speed testers.

3/ Subgroups 7 and 8 functional tests shall verify functionality of the device.

4/ * indicates PDA applies to subgroup 1 and 7. The PDA shall be based on the sum of the percent of die failures and the percent of non-die failures. The percent of die failures shall be determined by dividing the number of verified die failures by the total number of die in the lot initially submitted to burn-in. The percent of non-die failures shall be determined by dividing the number of verified non-die related failures by the total number of devices in the lot initially submitted to burn-in.

5/ ** see 4.4.1b

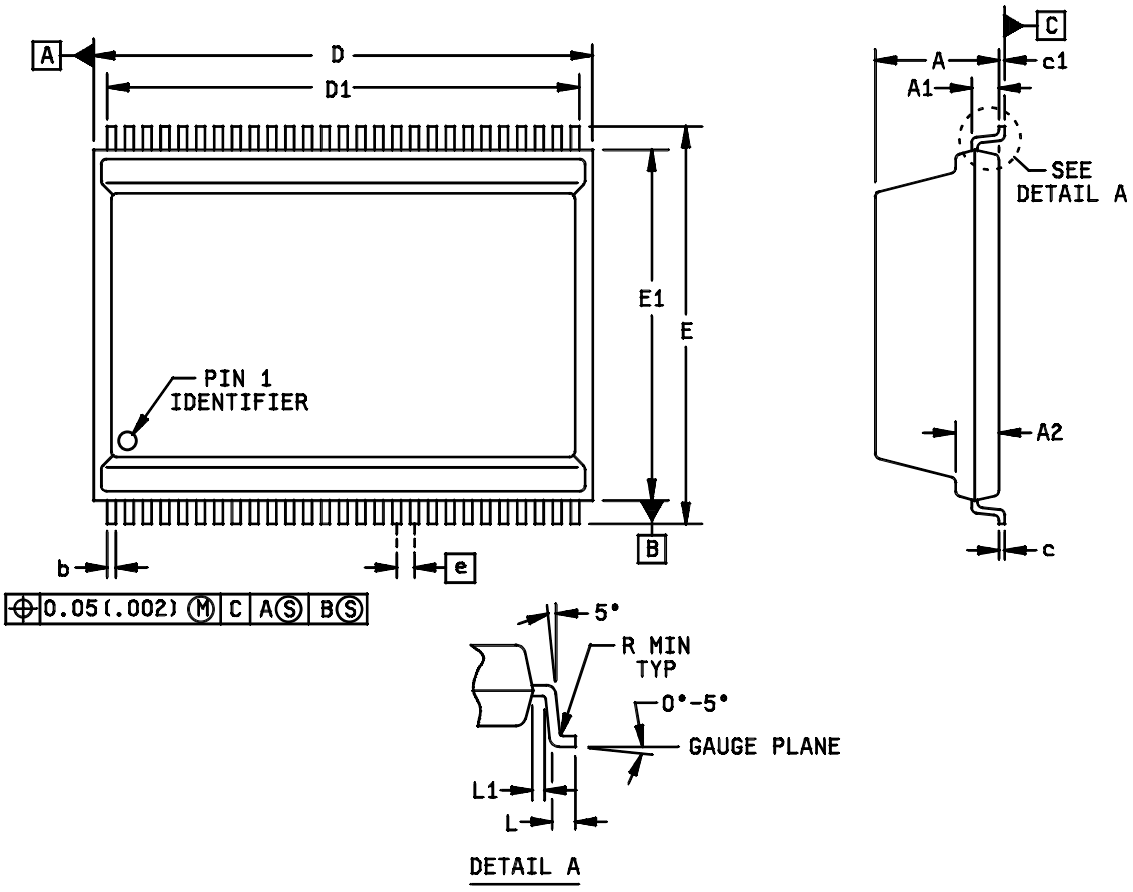
6/ Δ indicates delta limits shall be required (see table IIB) where specified, and the delta values shall be computed with reference to previous interim electrical parameters or as specified in the device manufacturer's QM plan. For device Class V, performance of delta limits shall be specified in the manufacturer's QM plan.

7/ Group A testing is not required if the requirements of MIL-PRF-38535 appendix B paragraph (B.4.2.a) has been accomplished.

Table IIB. Delta limits at +25°C.

Test 1/	All device types
I_I and I_O	± 10% of specified value in table I.
I_{CC3N}	± 10% of specified value in table I.

1/ The above parameter shall be recorded before and after the required burn-in and life tests to determine the delta.



Dimension		Millimeters		
		Min	Nom	Max
D		22.61	22.86	23.11
D1		21.13	21.18	21.23
E		16.90	17.15	17.40
E1		13.72	13.97	14.22
A	01 device			5.97
A1			1.26	
A2			2.57	

Dimension	Millimeters		
	Min	Nom	Max
b	0.33	0.38	0.43
e		0.80	
c	0.19	0.20	0.21
c1	0.20	0.25	0.30
L		0.84	
L1		0.64	
R	0.13		

Figure 1. Package Drawing Outline (Case X)

Device types	01	Device types	01
Case outlines	X	Case outlines	X
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	V_{CC}	28	V_{SS}
2	V_{CC}	29	A4
3	V_{CCQ}	30	A5
4	DQ4	31	A6
5	DQ0	32	A7
6	V_{SSQ}	33	A8
7	V_{SSQ}	34	A9
8	V_{SSQ}	35	A11
9	DQ5	36	A12
10	DQ1	37	CKE0
11	V_{CCQ}	38	CKE1
12	V_{CC}	39	CKE2
13	$\overline{WE}$	40	CKE3
14	$\overline{CAS}$	41	CLK1
		42	CLK2
15	$\overline{RAS}$	43	DQM
16	$\overline{CS3}$	44	V_{SS}
17	$\overline{CS2}$	45	V_{SSQ}
18	$\overline{CS1}$	46	DQ2
		47	DQ6
19	$\overline{CS0}$	48	V_{CCQ}
20	BA0	49	V_{CCQ}
21	BA1	50	DQ3
22	A10/AP	51	DQ7
23	A0	52	V_{SSQ}
24	A1	53	V_{SS}
25	A2	54	V_{SS}
26	A3		
27	V_{CC}		

FIGURE 2. Terminal connections .

PIN	NAME	INPUT FUNCTION
CLK1, CLK2	System Clock	Active on the positive going edge to sample all inputs
$\overline{CSO}$ ~ $\overline{CS}$**3**	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK, CKE. and DQM
CKE0 ~ CKE3	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A12	Address	Row / Column addresses are multiplexed on the same pins. Row address: RA0~RA12, column address: CA0 ~ CA9, CA11
BA0 ~ BA1	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	Data Input/Output Mask	Makes data output Hi-Z, tshz, after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ 7	Data Input/Output	Data inputs/outputs are multiplexed on the same pins.
V_{CC}/V_{SS}	Power Supply/Ground	Power and ground for the input buffers and the core logic.
V_{CCQ}/V_{SSQ}	Data Output Power/Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left open. No Connection on the device.

FIGURE 2. Terminal connections Continued.

Command			CKE_{n-1}	CKE_n	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	$BA_{0,1}$	A_{10}/AP	A_{11}, A_{12} A_9 ~ A_0	Note
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row address			H	X	L	L	H	H	X	V	Row address		
Read & Column Address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column Address A_0 ~ A_9, A_{11}	4
	Auto precharge enable										H		4,5
Write & Column Address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column Address A_0 ~ A_9, A_{11}	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

(V = Valid, X = Don't care, H = Logic high, L = Logic low)

Notes:
1. OP Code : Operand code
   A_0 ~ A_{12} & BA_0 ~ BA_1 : Programs keys, (@ MRS)
2. MRS can be issued only at all banks precharge state
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM
   The automatical precharge without low precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA_0 ~ BA_1: Bank select addresses.
   If both BA_0 and BA_1 are "Low" at read, write, row active and precharge, bank A is selected.
   If both BA_0 is "High" and BA_1 is "Low" at read, write, row active and precharge, bank B is selected.
   If both BA_0 is "Low" and BA_1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA_0 and BA_1 are "High" at read, write, row active and precharge, bank D is selected.
   If A_{10}/AP is "High" at row precharge, BA_0 and BA_1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command cannot be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at t_{RP} after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0) but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)

FIGURE 3. Truth table and device operations.

A. MODE REGISTER FIELD TABLE TO PROGRAM MODES

Register Programmed with MRS

Address	BA_0 ~ BA_1	A_{12} ~ A_{10}/AP	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0
Function	RFU	RFU	W.B.L.	TM		CAS Latency			BT	Burst Length		

Test Mode			CAS Latency				Burst Type		Burst Length				
A_8	A_7	Type	A_6	A_5	A_4	Latency	A_3	Sequential	A_2	A_1	A_0	BT = 0	BT = 1
0	0	Mode Register Set	0	0	0	Reserved	0	Sequential	0	0	0	1	1
0	1	Reserved	0	0	1	Reserved	1	Interleave	0	0	1	2	2
1	0	Reserved	0	1	0	2			0	1	0	4	4
1	1	Reserved	0	1	1	3			0	1	1	8	8
Write Burst Length			1	0	0	Reserved			1	0	0	Reserved	Reserved
A_9	Length		1	0	1	Reserved			1	0	1	Reserved	Reserved
0	Burst		1	1	0	Reserved			1	1	0	Reserved	Reserved
1	Single Bit		1	1	1	Reserved			1	1	1	Full Page	Reserved

***Full Page Length**
64Mb : x4 (1024), x8 (512), x 16 (256)
128Mb : x4 (2048), x8 (1024), x 16 (512)
256Mb : x4 (2048), x8 (1024), x 16 (512)

B POWER UP SEQUENCE

1. Apply power and start clock, attempt to maintain CKE = "H", DQM = "H" and other pins are NOP condition at the inputs.
2. Maintain stable power, stable clock and NOP input condition for a minimum of 200µs.
3. Issue precharge commands for all banks of the devices.
4. Issue 2 or more auto-refresh commands.
5. Issue a mode register set command to initialize the mode register.
   Sequence of 4 & 5 is regardless of the order. The device is now ready for normal operation.

Note:
1. If A_9 is high during MRS cycle, "Burst Read Single Bit Write" function will be enabled.
2. RFU (Reserved for future use) should stay "0" during MRS cycle.

C. BURST SEQUENCE

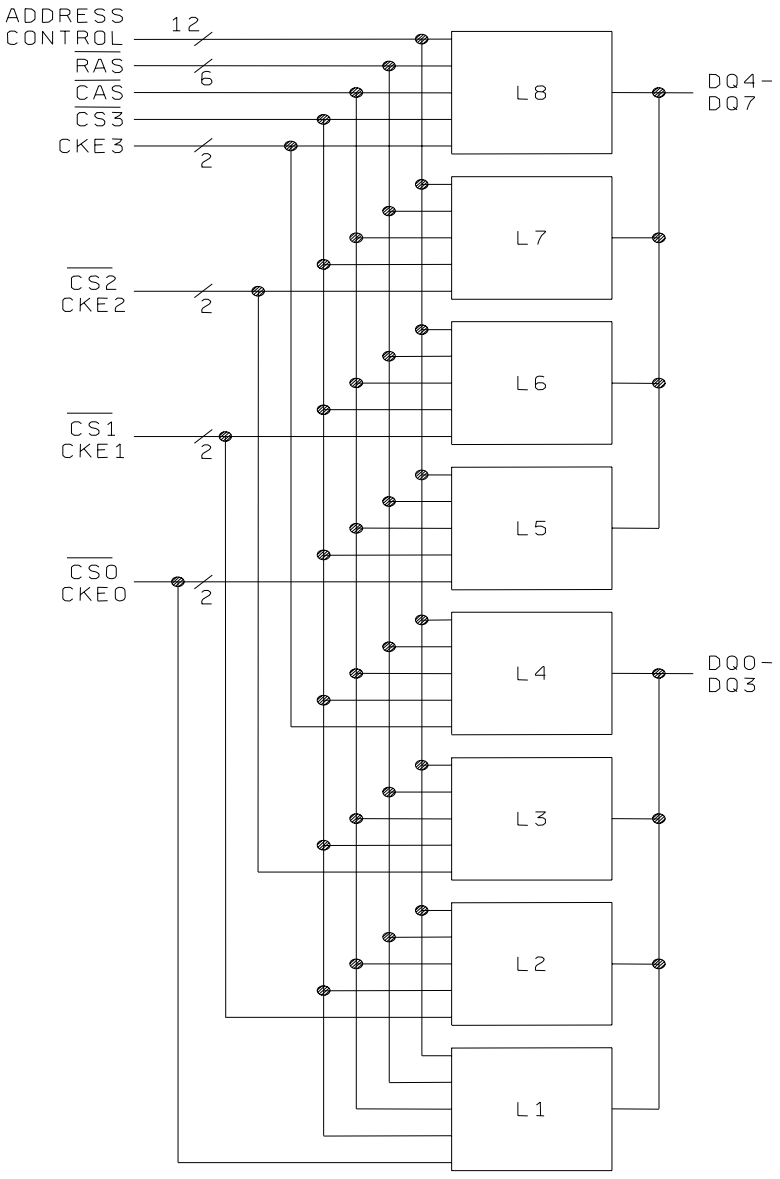
1. BURST LENGTH = 4

Initial Address		Sequential				Interleave			
A_1	A_0								
0	0	0	1	2	3	0	1	2	3
0	1	1	2	3	0	1	0	3	2
1	0	2	3	0	1	2	3	0	1
1	1	3	0	1	2	3	2	1	0

2. BURST LENGTH = 8

Initial Address			Sequential								Interleave							
A_2	A_1	A_0																
0	0	0	0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7
0	0	1	1	2	3	4	5	6	7	0	1	0	3	2	5	4	7	6
0	1	0	2	3	4	5	6	7	0	1	2	3	0	1	6	7	4	5
0	1	1	3	4	5	6	7	0	1	2	3	2	1	0	7	6	5	4
1	0	0	4	5	6	7	0	1	2	3	4	5	6	7	0	1	2	3
1	0	1	5	6	7	0	1	2	3	4	5	4	7	6	1	0	3	2
1	1	0	6	7	0	1	2	3	4	5	6	7	4	5	2	3	0	1
1	1	1	7	0	1	2	3	4	5	6	7	6	5	4	3	2	1	0

FIGURE 3. Truth table and device operations Continued.



L1 through L8 are 64M x 4 SDRAM

Figure 4a. Functional block diagram

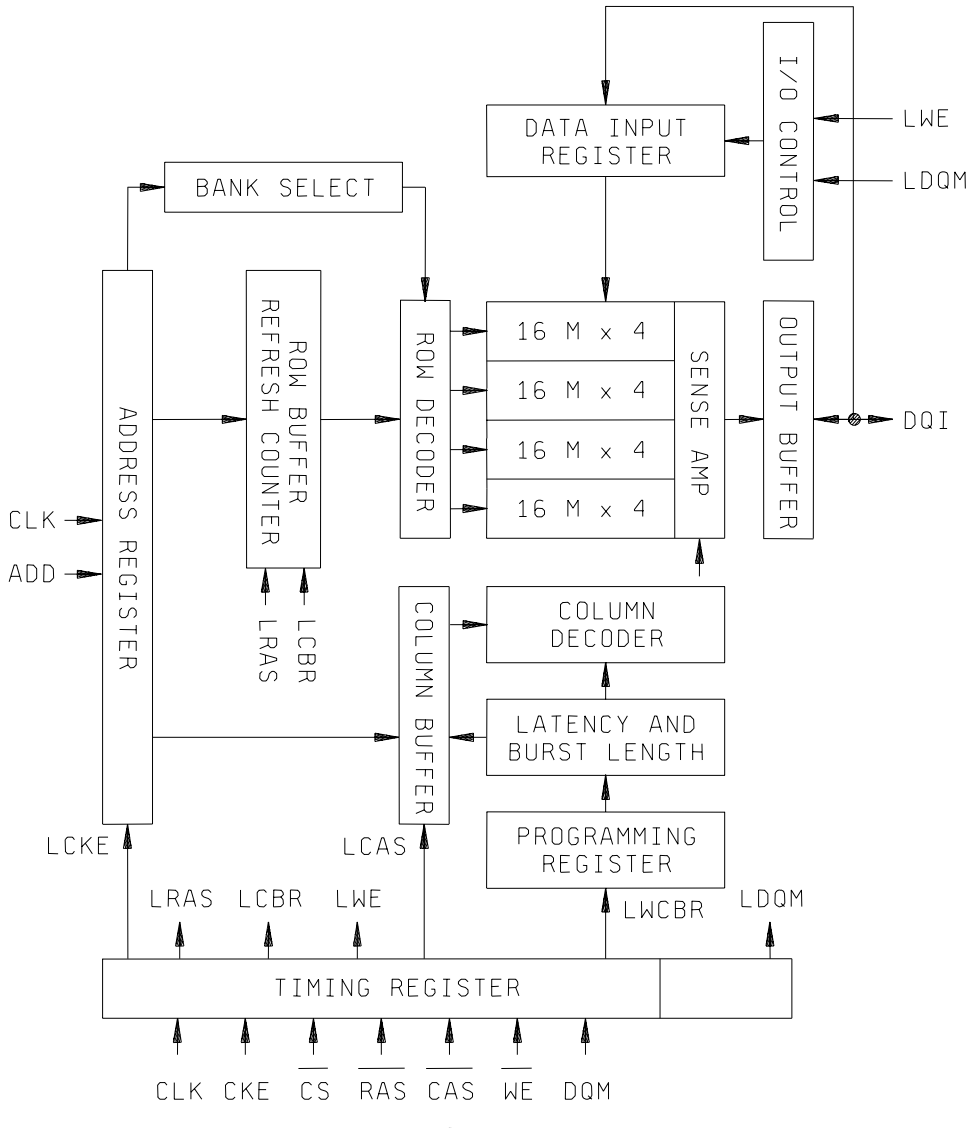


Figure 4b. Functional block diagram (Per Die)

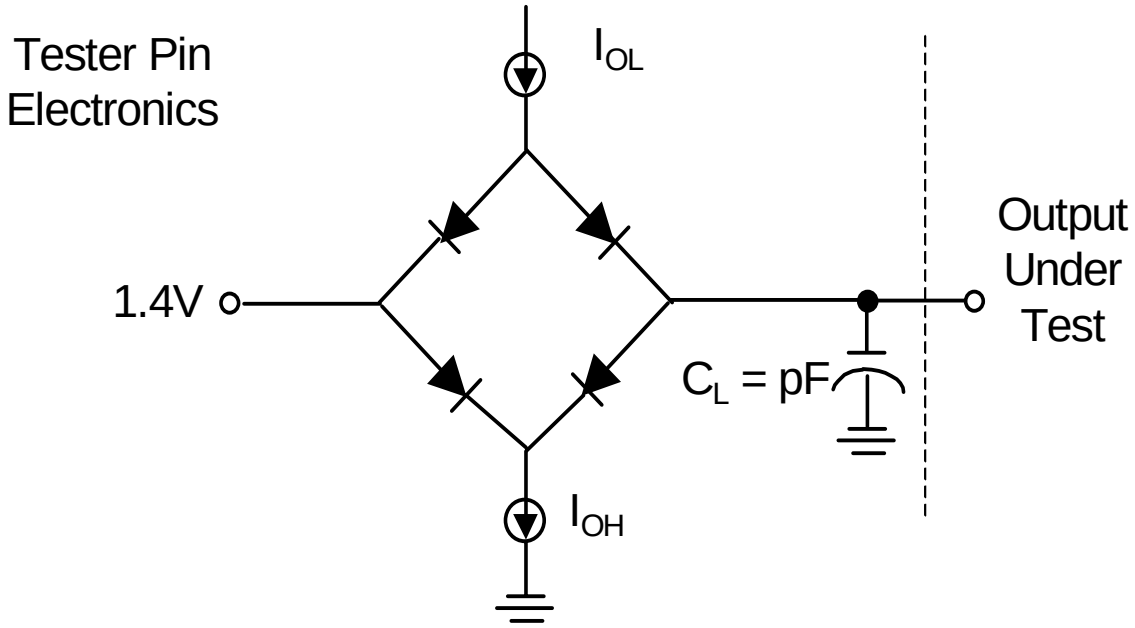
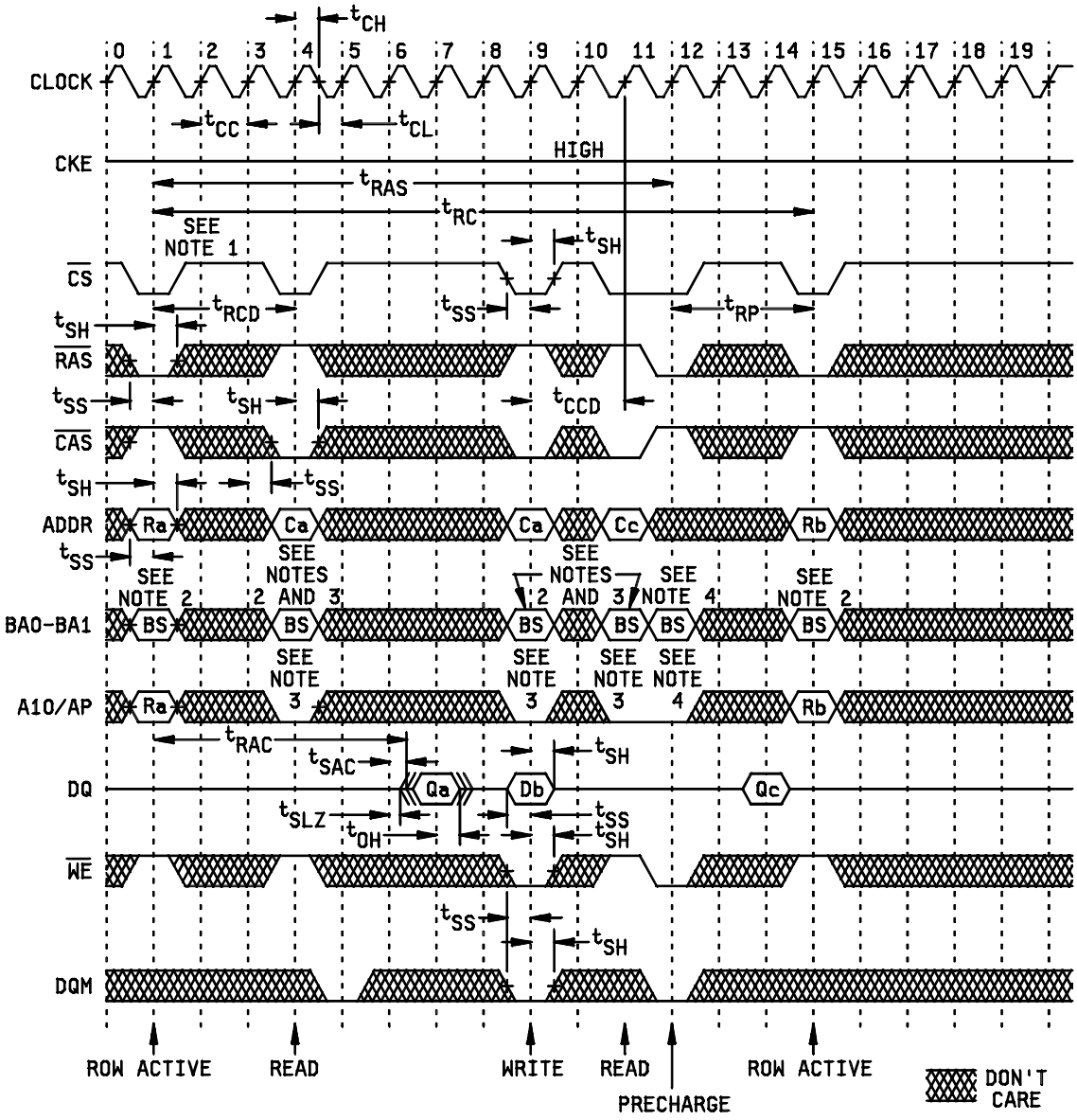


Figure 4c. Output load circuit.



SINGLE BIT READ-WRITE-READ CYCLE(SAME PAGE)@CAS LATENCY=3, BURST LENGTH=1

Notes: See notes on next page.

FIGURE 5. Timing waveforms.

1. All input except CKE & DQM can be don't care when $\overline{CS}$ is high at the CLK high going edge.
2. Bank active & Read/Write are controlled by BA_0~ BA_1.

BA_0	BA_1	Active & Read/Write
0	0	Bank A
0	1	Bank B
1	0	Bank C
1	1	Bank D

Notes continued on next page.

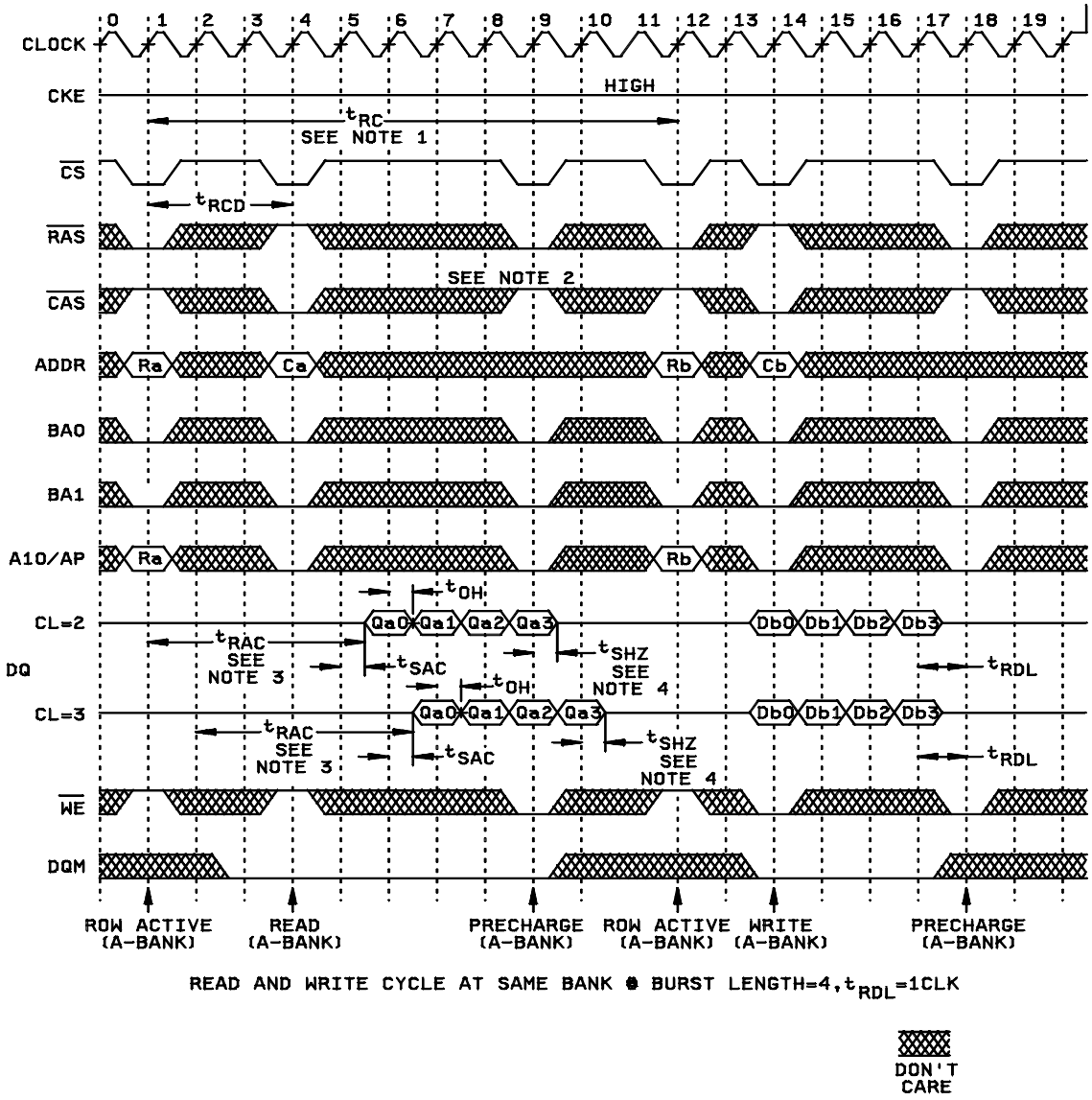
3. Enable and disable auto precharge function are controlled by A10/AP in Read/Write command.

A10/AP	BA_0	BA_1	Operation
0	0	0	Disable auto precharge, leave Bank A active at end of burst.
	0	1	Disable auto precharge, leave Bank B active at end of burst.
	1	0	Disable auto precharge, leave Bank C active at end of burst.
	1	1	Disable auto precharge, leave Bank D active at end of burst.
1	0	0	Enable auto precharge, leave Bank A active at end of burst.
	0	1	Enable auto precharge, leave Bank B active at end of burst.
	1	0	Enable auto precharge, leave Bank C active at end of burst.
	1	1	Enable auto precharge, leave Bank D active at end of burst.

4. A10/AP and BA_0~ BA_1 control bank precharge when precharge command is asserted.

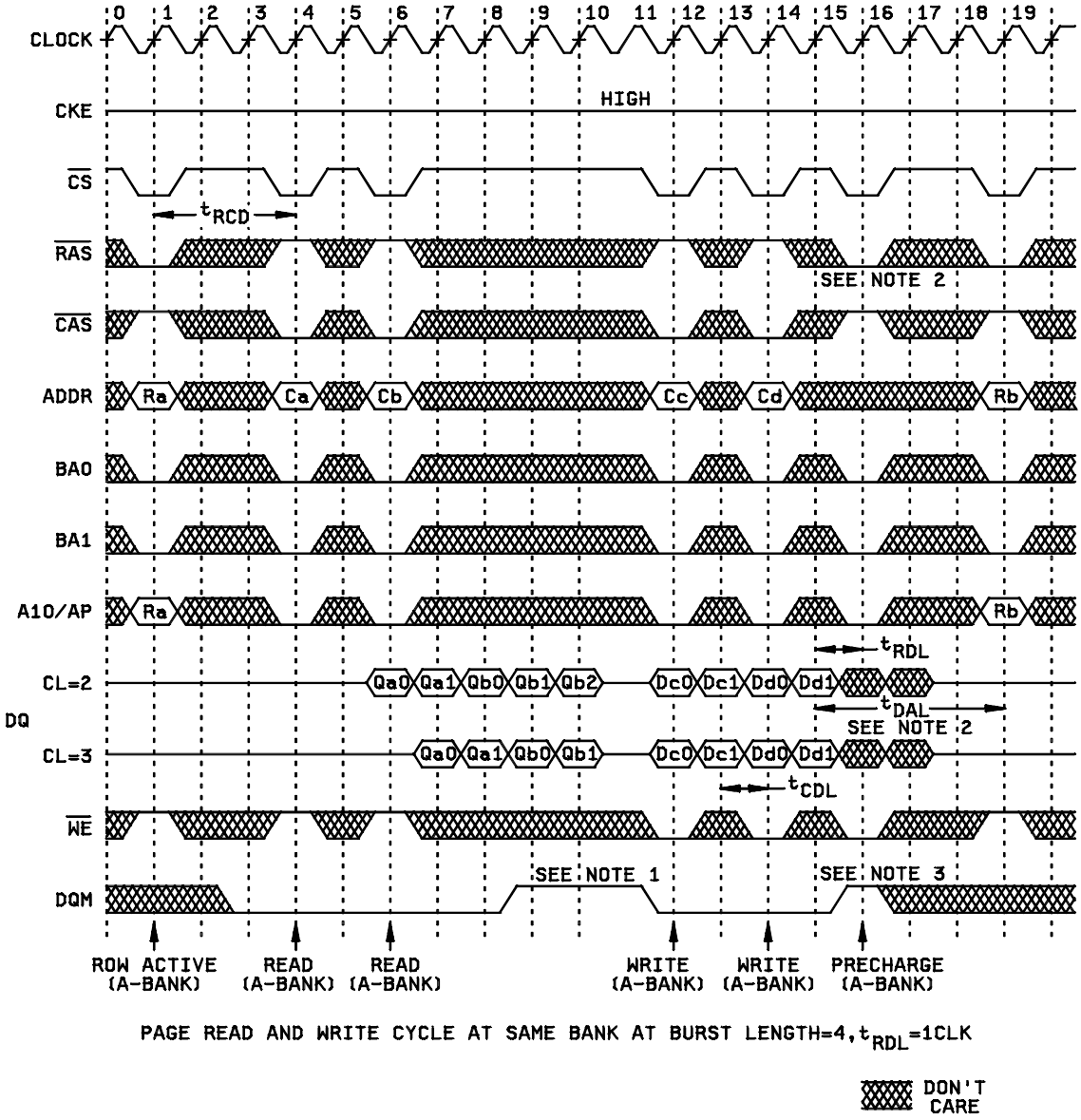
A10/AP	BA_0	BA_1	Precharge
0	0	0	Bank A
0	0	1	Bank B
0	1	0	Bank C
0	1	1	Bank D
1	X	X	All Banks

FIGURE 5. Timing waveforms Continued.



Notes: 1. Minimum row cycle times is required to complete internal DRAM operation
2. Row precharge can interrupt burst on any cycle. [CAS Latency - 1] number of valid output data is available after Row precharge. Last valid output will be Hi-Z(t_{SHZ}) after the clock.
3. Access time from Row active command. TCC *(t_{RCD} + CAS latency - 1) + t_{SAC}.
4. Output will be HI-Z after the end of burst . (1,2,4,8 &Full page bit burst)

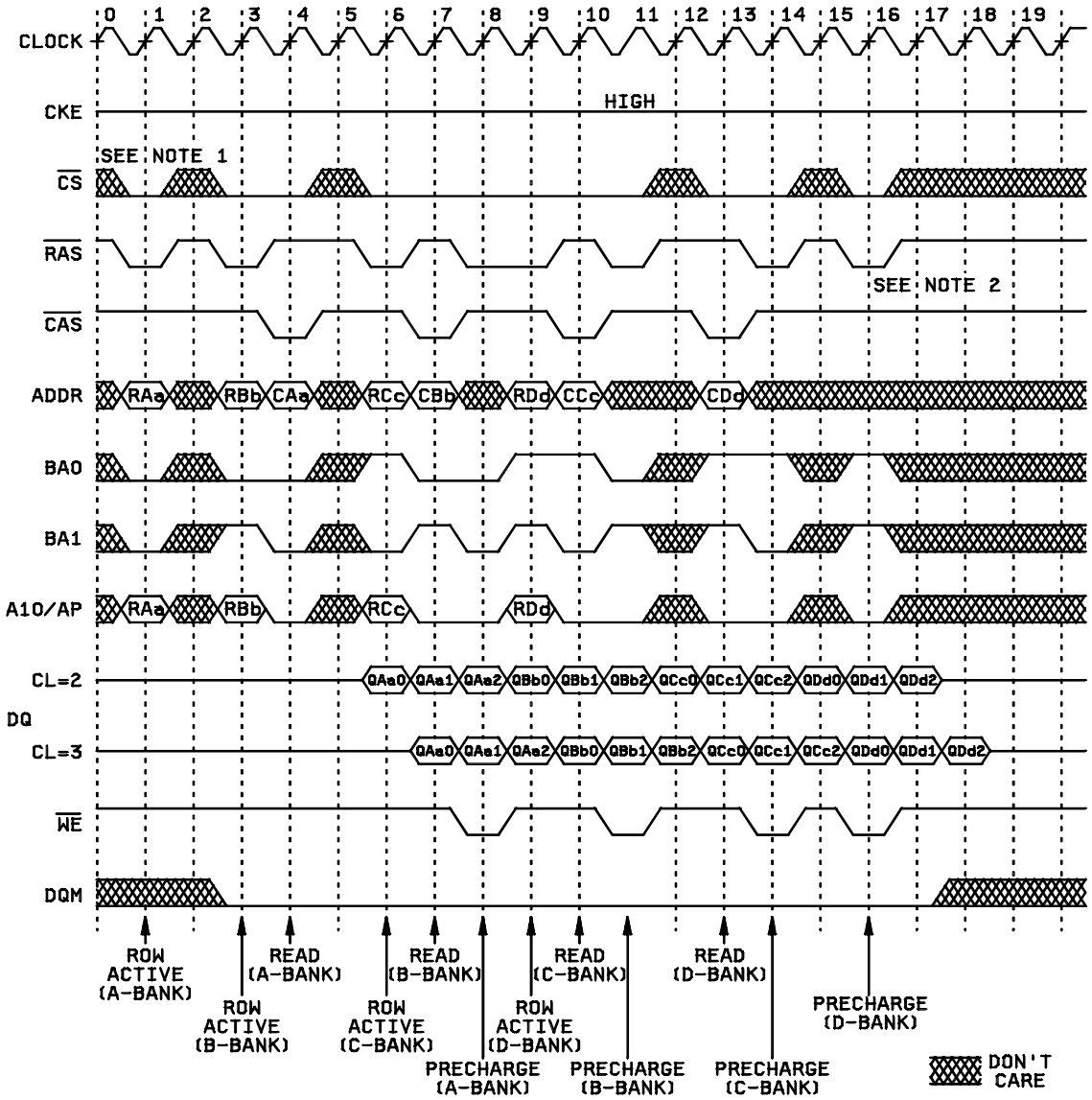
FIGURE 5. Timing waveforms Continued.



Notes:

1. To write data before burst read ends, DQM should be asserted three cycles prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge will be written.
3. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
4. t_{DAL}, last data in to active delay, is 1CLK + 20 ns.

FIGURE 5. Timing waveforms Continued.

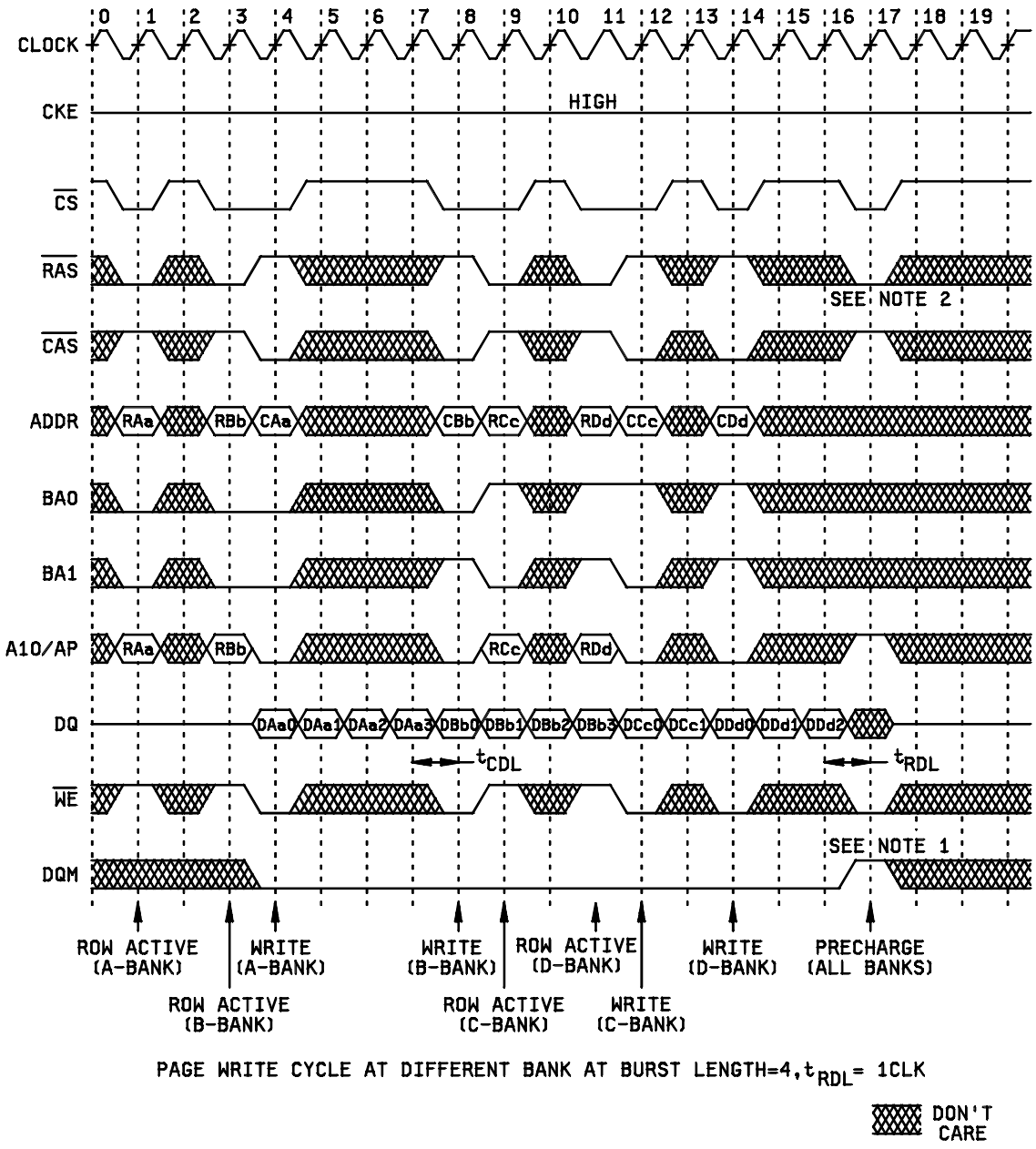


PAGE READ CYCLE AT DIFFERENT BANK AT BURST LENGTH = 4

Notes:

1. $\overline{CS}$. Can be don't care when $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ are high at the clock high going edge.
2. To interrupt a burst read by row precharge, both the read and the precharge banks must be the same.

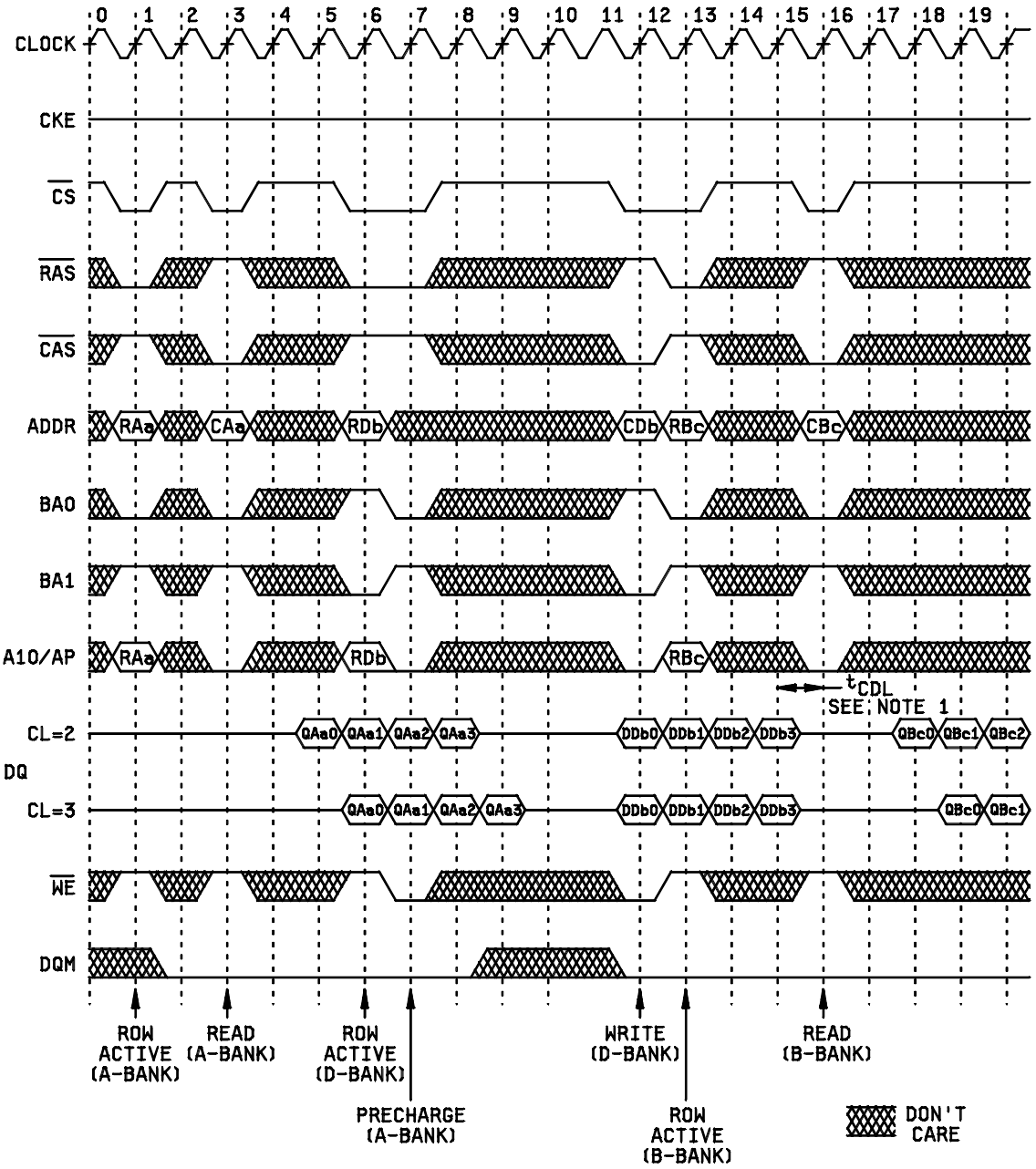
FIGURE 5. Timing waveforms Continued.



Notes:

1. To interrupt burst write by Row precharge, DQM should be asserted to mask invalid input data.
2. To interrupt burst write by Row precharge, both the write and the precharge banks must be the same.

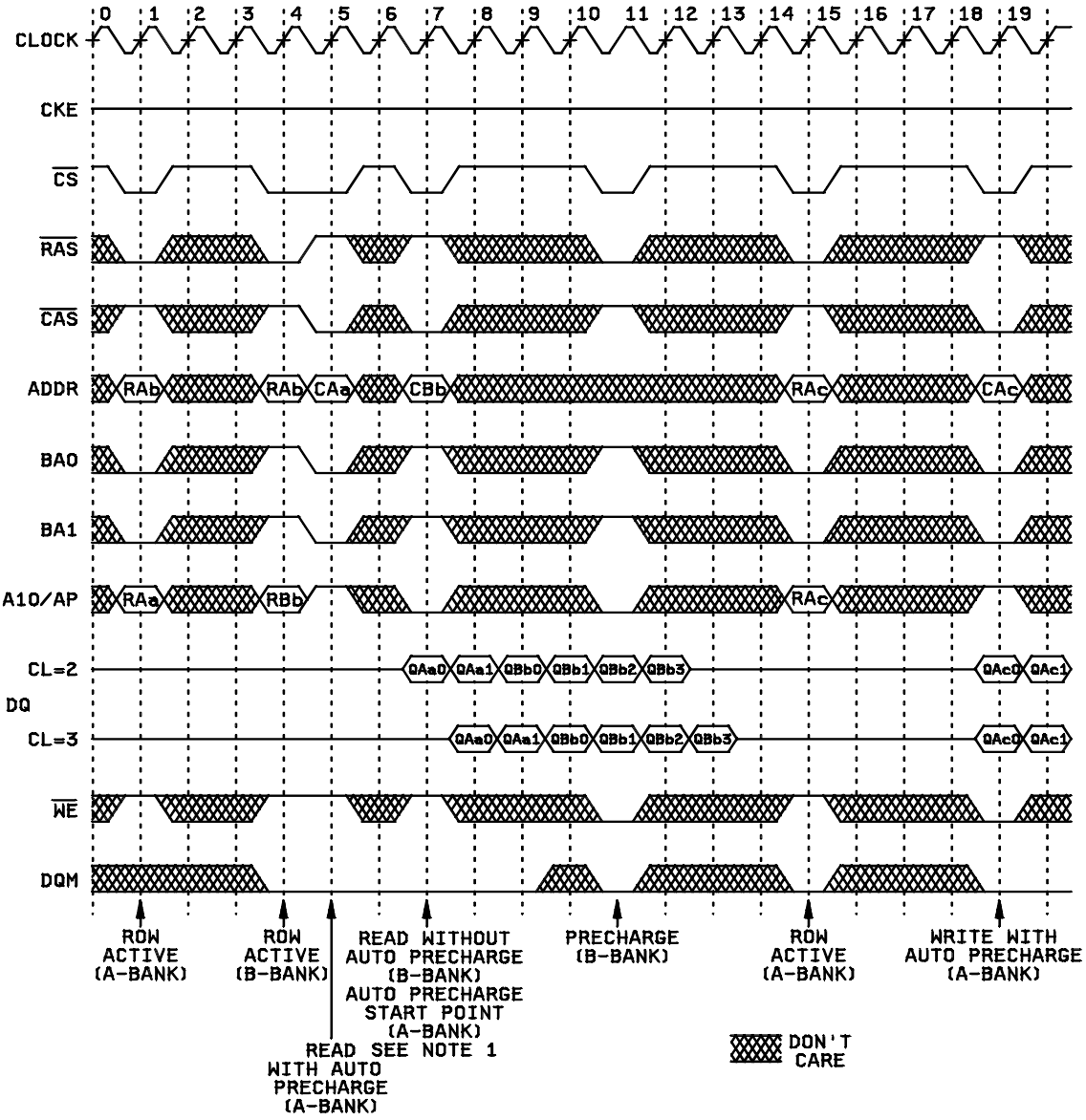
FIGURE 5. Timing waveforms Continued.



READ AND WRITE CYCLE AT DIFFERENT BANK AT BURST LENGTH = 4

Note 1: t_{CDL} should be met to complete write.

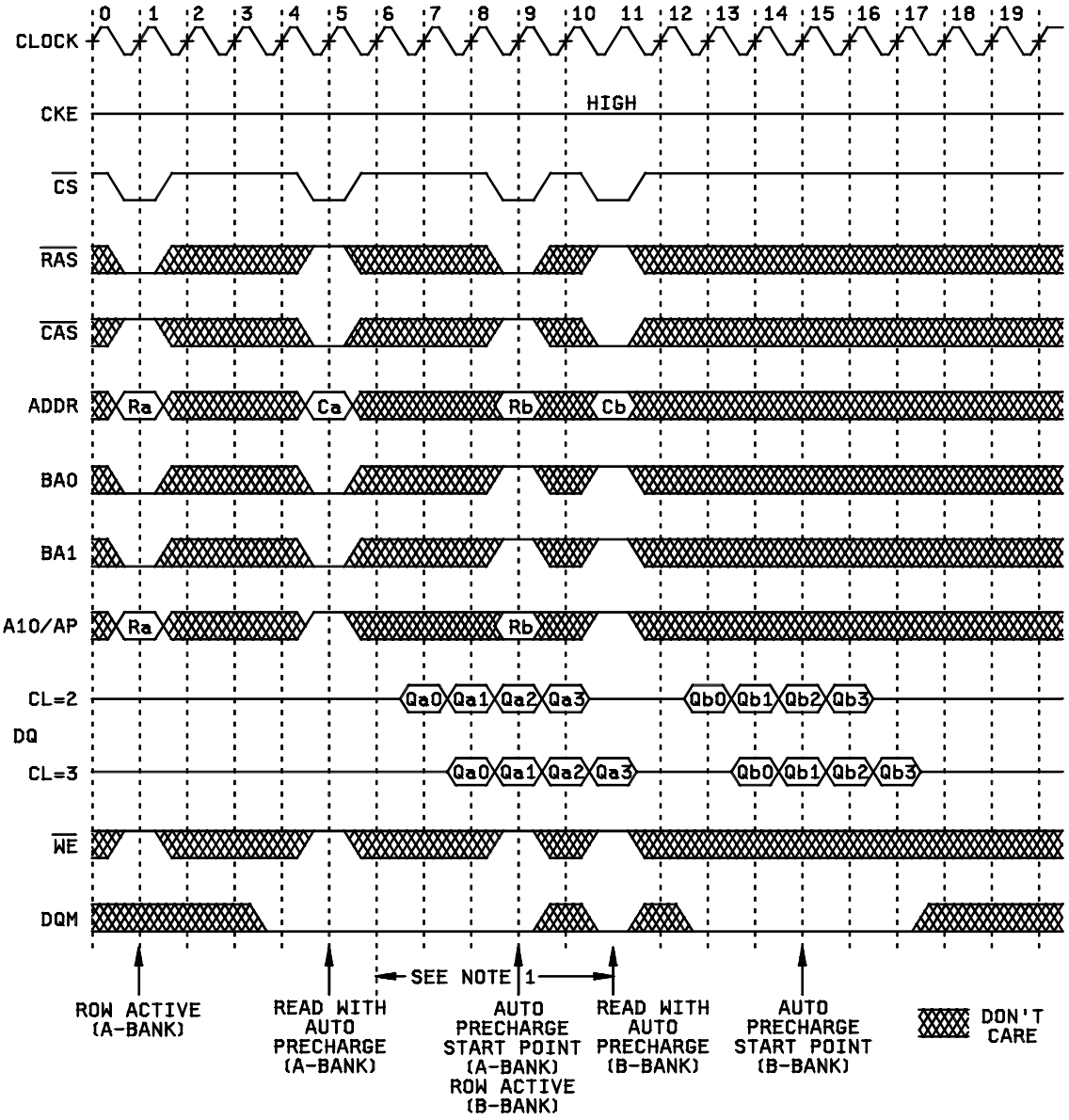
FIGURE 5. Timing waveforms Continued.



READ AND WRITE CYCLE WITH AUTO PRECHARGE 1 AT BURST LENGTH = 4

Note 1: When Read(Write) command with auto precharge is issued at A-Bank after A and B Bank activation:
If Read(Write) command without auto precharge is issued at B-Bank before A-Bank auto precharge starts, A-Bank Auto precharge will start at B-Bank read command input point.
Any command can not be issued at A-Bank during t_{RP} after A-Bank auto precharge starts.

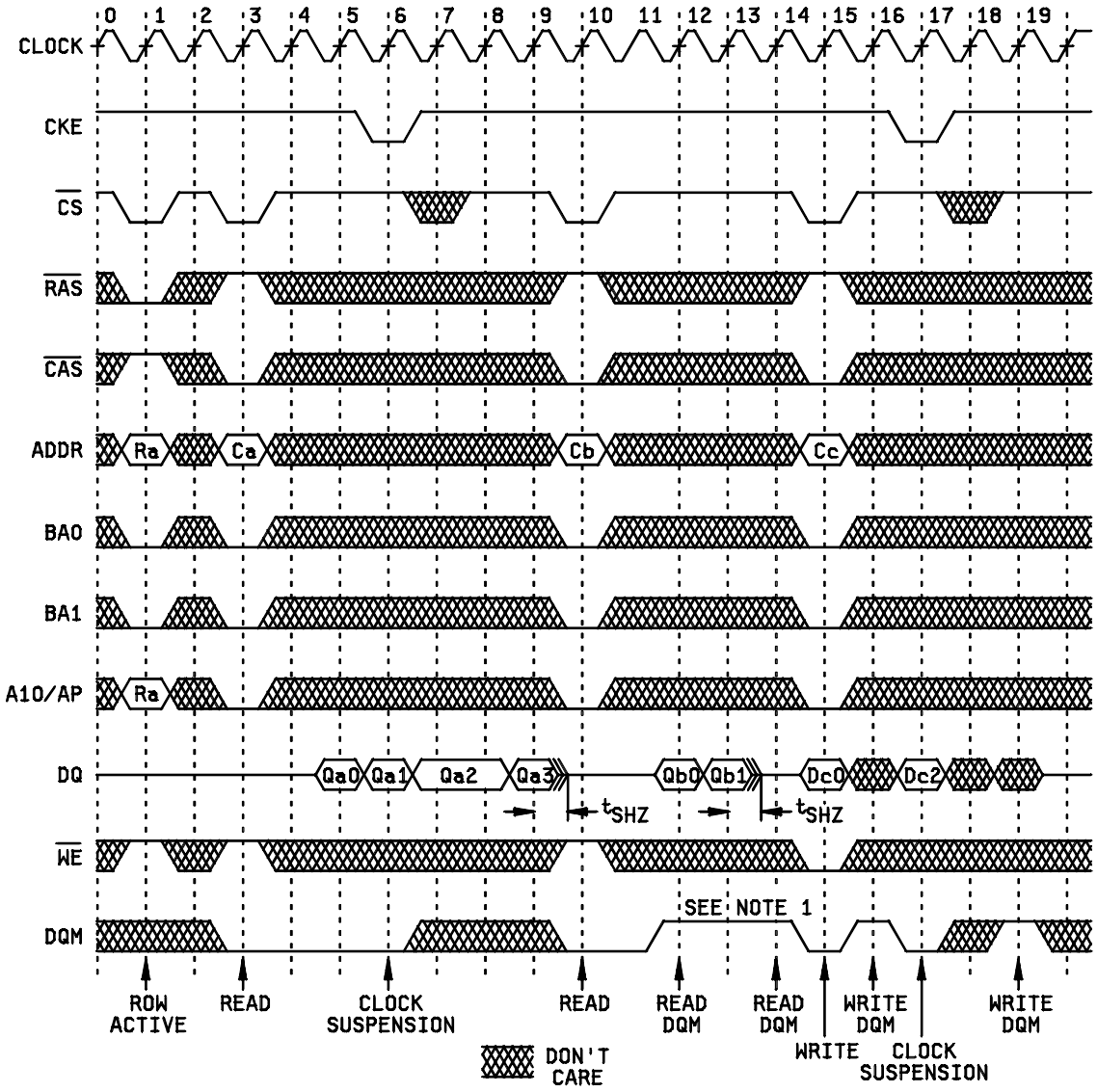
FIGURE 5. Timing waveforms Continued.



READ AND WRITE CYCLE WITH AUTO PRECHARGE II AT BURST LENGTH = 4

Note 1: Any command to A-Bank is not allowed in this period. t_{RP} is determined from at auto precharge start point.

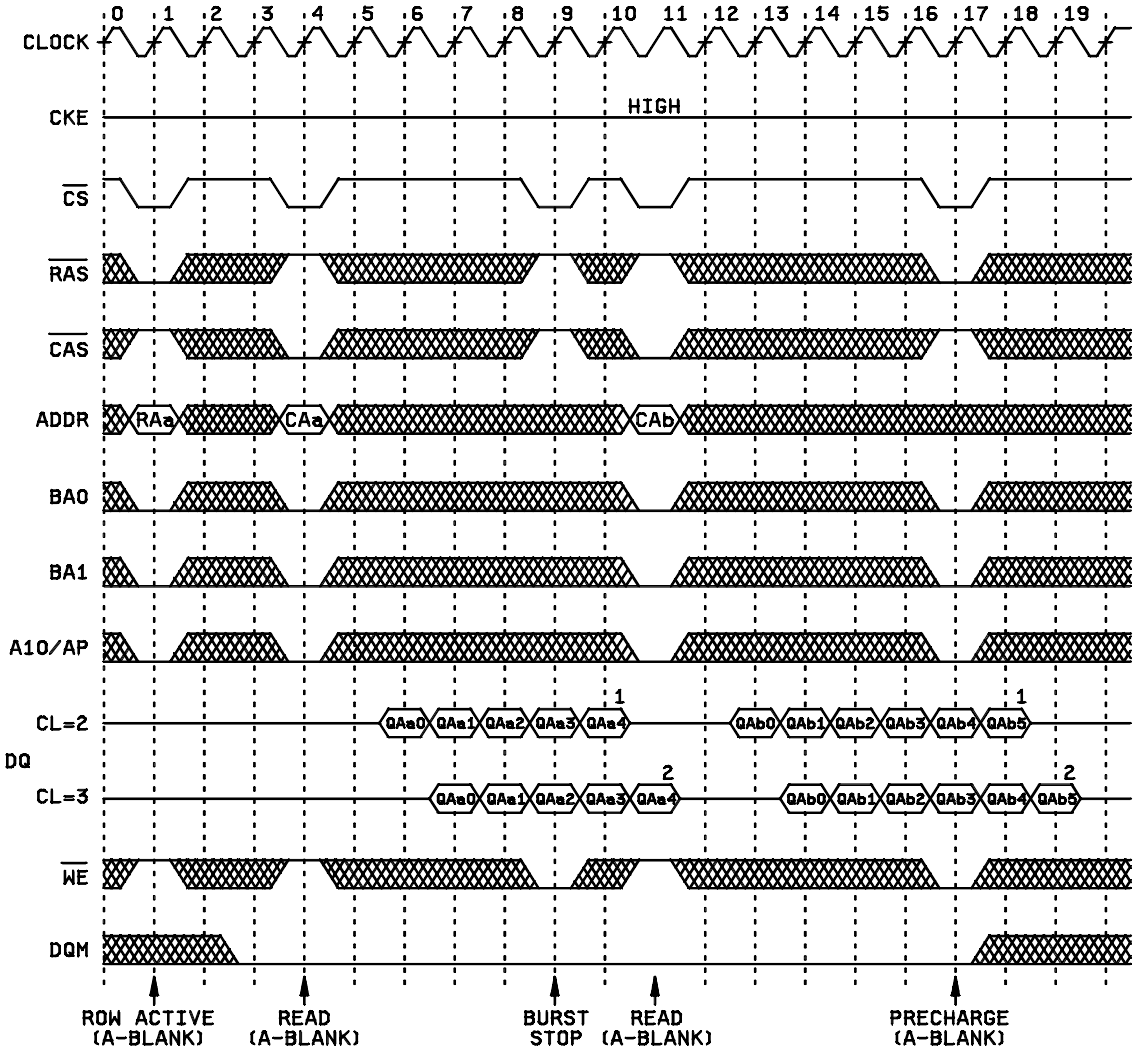
FIGURE 5. Timing waveforms Continued.



CLOCK SUSPENSION AND DQM OPERATION CYCLE AT CAS LATENCY=2, BURST LENGTH=4

Note 1: DQM is needed to prevent bus contention.

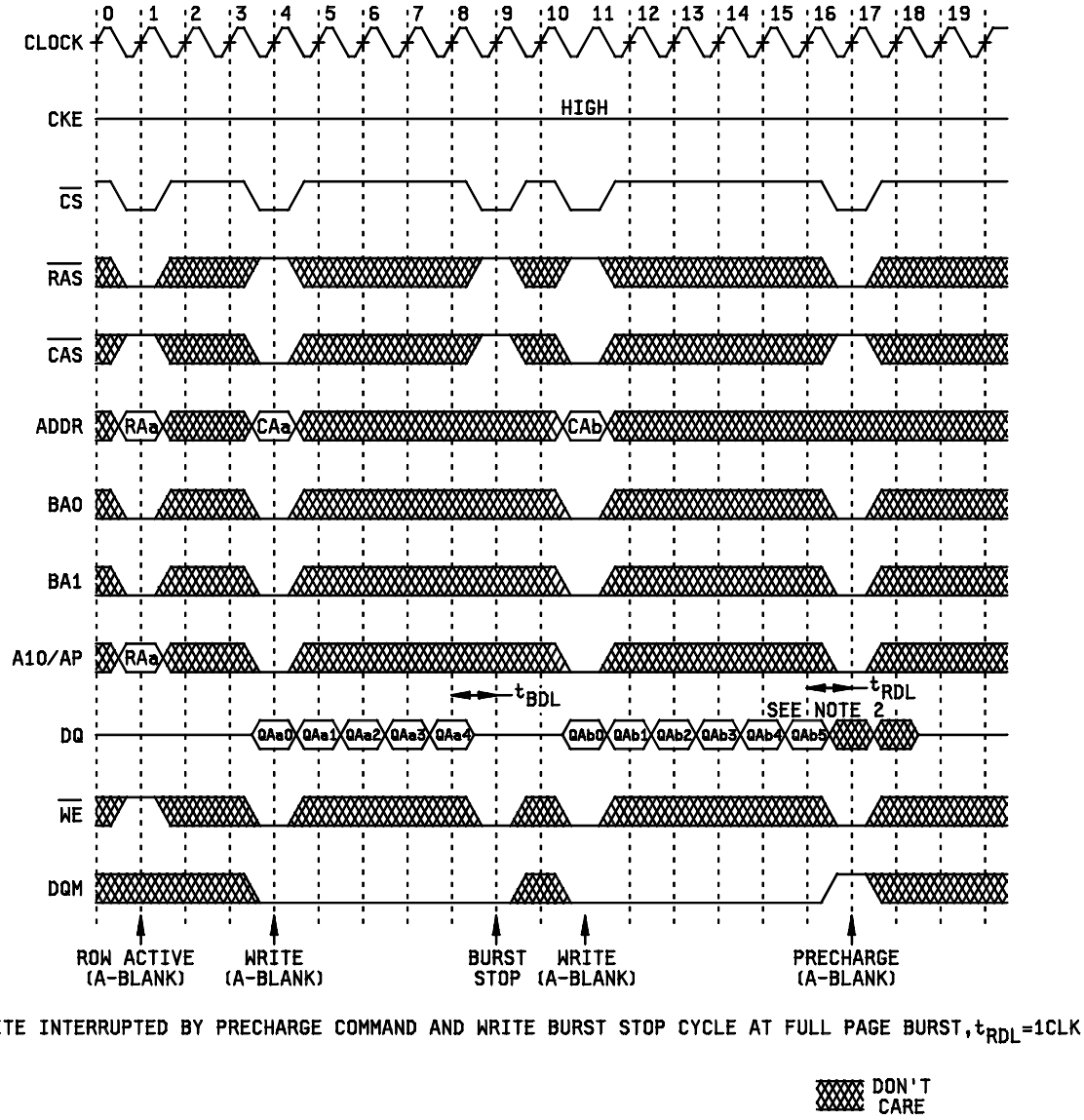
FIGURE 5. Timing waveforms Continued.



Notes:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is same as the case of $\overline{\text{RAS}}$ interrupt. Both cases are illustrated above in timing diagram, See label 1,2; but at burst write, burst stop and $\overline{\text{RAS}}$ interrupt should be compared carefully. Refer to the timing diagram of “Full page write burst stop cycle”.
3. Burst stop is valid at every burst length.

FIGURE 5. Timing waveforms Continued.

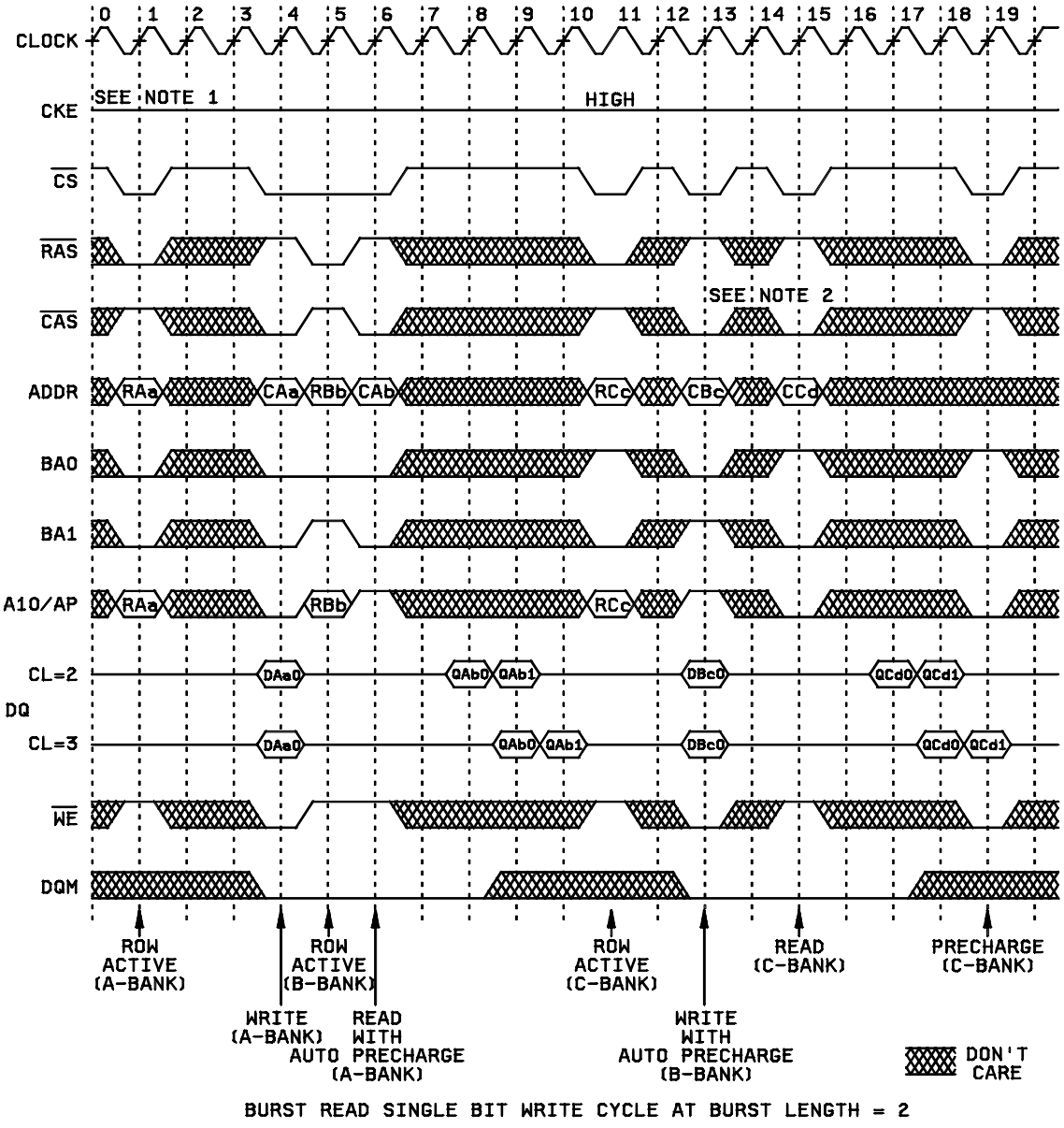


WRITE INTERRUPTED BY PRECHARGE COMMAND AND WRITE BURST STOP CYCLE AT FULL PAGE BURST, t_{RDL}=1CLK

Notes:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   DQM at write interrupted by precharge command is needed to prevent invalid write. DQM should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

FIGURE 5. Timing waveforms Continued.

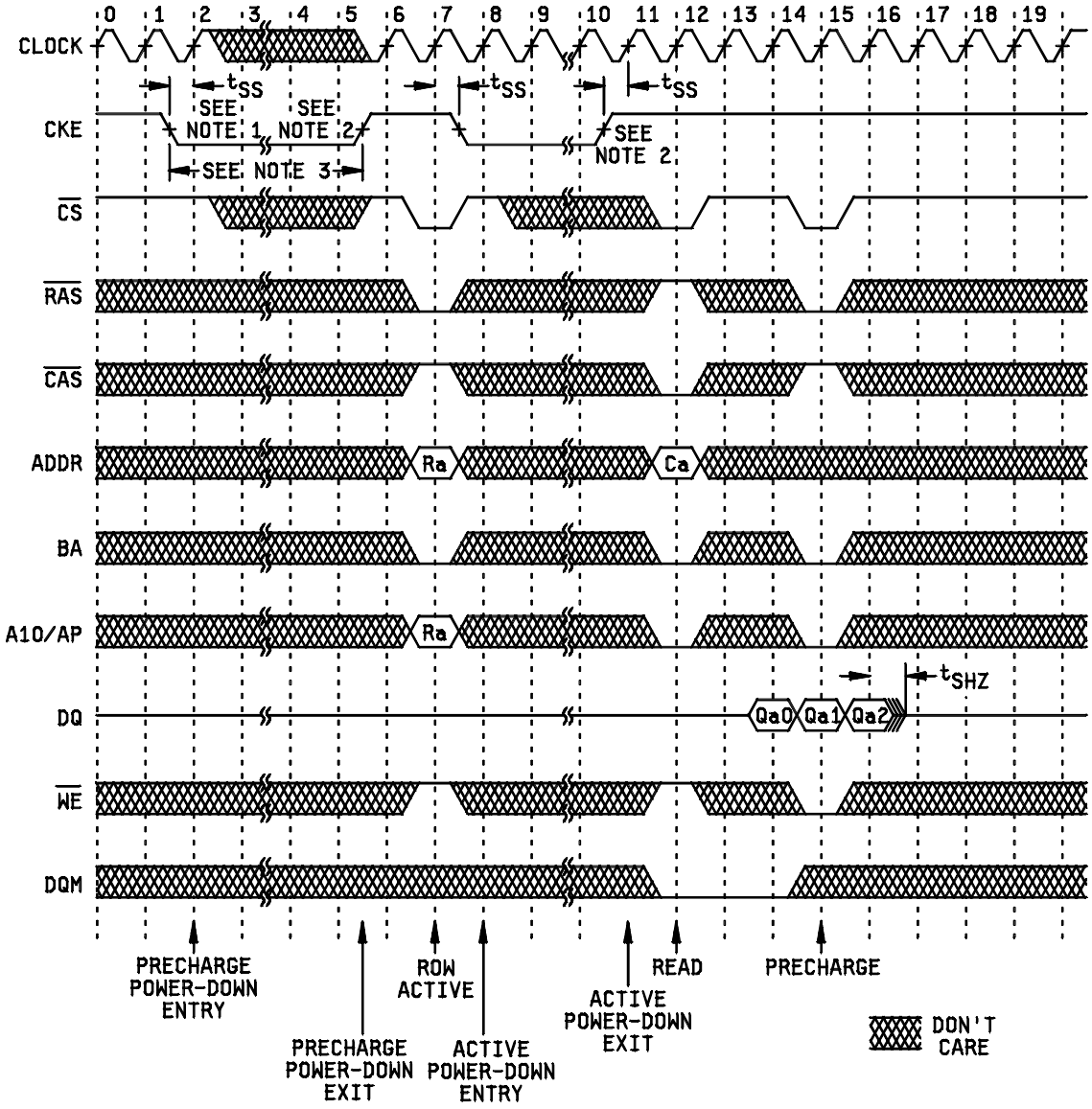


BURST READ SINGLE BIT WRITE CYCLE AT BURST LENGTH = 2

Notes:

1. BRSW modes is enabled by setting A9 “High” at MRS(Mode Register Set). At the BRSW Mode the burst length at write is fixed to “1” regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep in mind that t_{RAS} should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

FIGURE 5. Timing waveforms Continued.

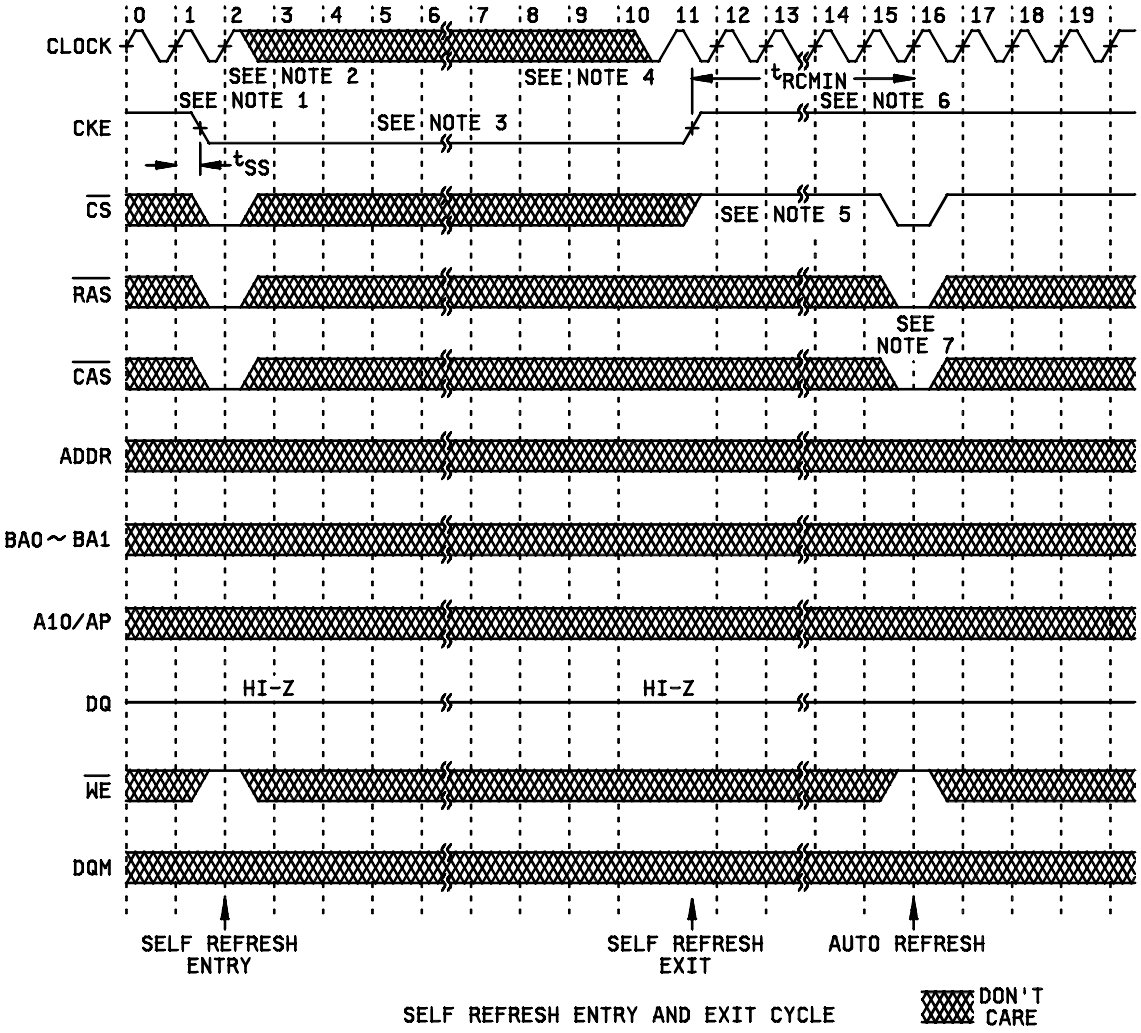


ACTIVE/PRECHARGE POWER DOWN MODE AT CAS LATENCY = 2, BURST LENGTH = 4

Notes:

1. Both banks should be in idle state prior to entering precharge power down mode.
2. CKE should be set high at least 1CLK +t_{SS} prior to Row active command.
3. Can not violate minimum refresh specification. (64 ms).

FIGURE 5. Timing waveforms Continued.



SELF REFRESH ENTRY AND EXIT CYCLE

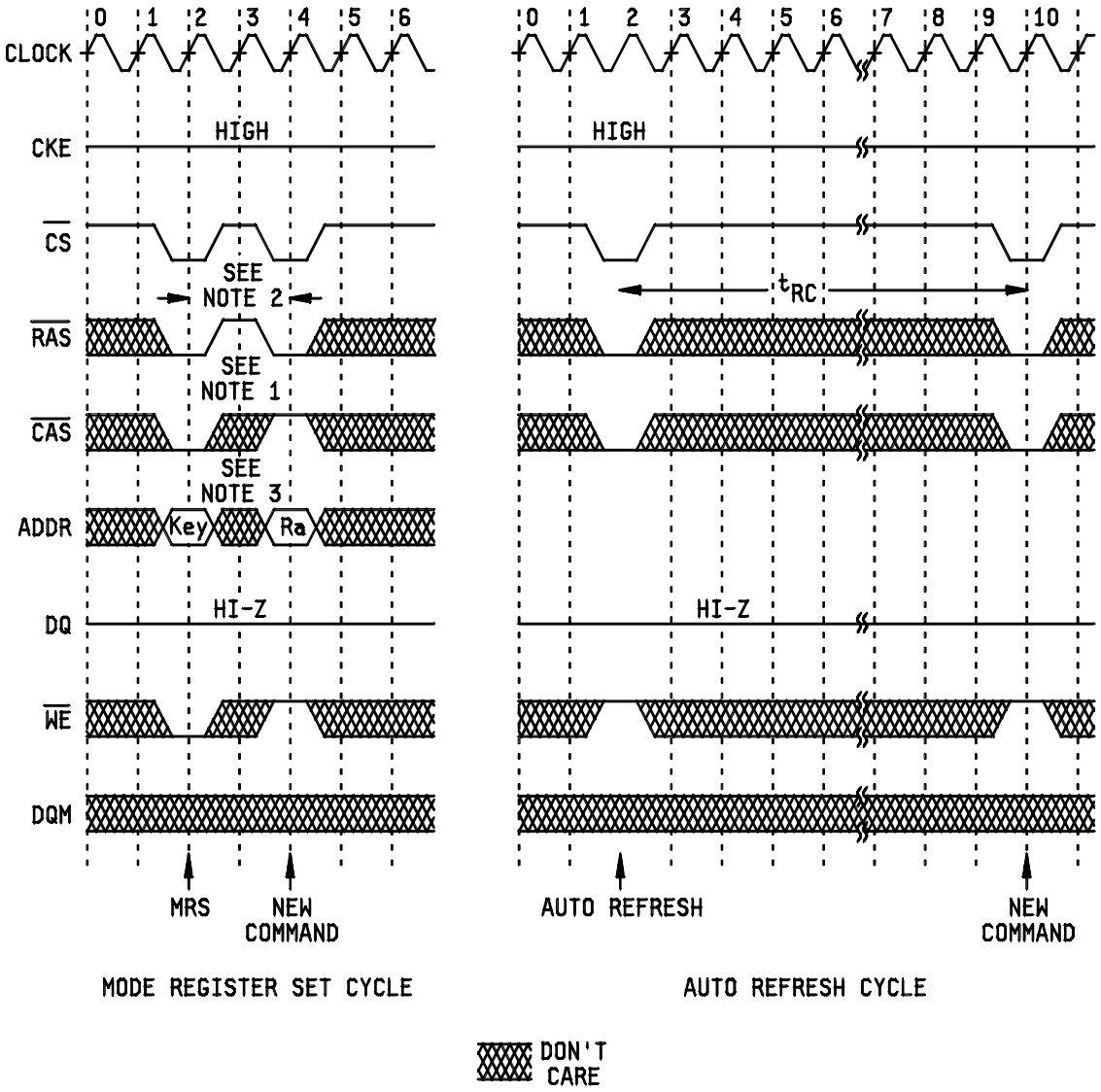
Notes: TO ENTER SELF REFRESH MODE

1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, with CKE should be low at the same clock cycle.
2. After 1 clock cycle, all the inputs including the system clock can be don't care except for CKE.
3. The device remains in self refresh mode as long as CKE stays "low". Once the device enters self refresh mode minimum t_{RAS} is required before exit from self refresh.

TO EXIT SELF REFRESH MODE

4. System clock restart and be stable before returning CKE high.
5. $\overline{CS}$ starts from high.
6. Minimum t_{RC} is required after CKE going high to complete self refresh exit.
7. 4K cycle(64 Mb 5th, 128 Mb 2nd/3rd) or 8K cycle (256 Mb 2nd) of burst auto refresh is required before self refresh entry and after self refresh exit if the system uses burst refresh.

FIGURE 5. Timing waveforms Continued.



*All banks precharge should be completed before Mode Register Set cycle and auto refresh cycle.

Notes:

1. $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, and $\overline{WE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{RAS}$ activation.
3. Please refer to Mode Register Set table.

FIGURE 5. Timing waveforms Continued.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes N, Q, and V.

5.2 Special Class N handling. Class N device is rated as a Moisture Sensitivity Level 3 part when tested per J-STD-020A. Device will be baked and dry packed when shipped from the manufacturer. Device will require a 125°C dry bake for 24 hours prior to installation if prolonged exposure on normal factory floor of the end user has occurred.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes N, Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 03 – 02 – 07

Approved sources of supply for SMD 5962-02518 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-0251801NXA	0CET3	SD256Mx88
5962-0251801NXB	0CET3	SD256Mx88

1/ The lead finish shown for each PIN representing the most readily available finish from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
0CET3	Vertical Circuits Incorporated 19951 Mariner Avenue Torrance, CA 90503